WHAT IS CLAIMED IS:

1. An amplifier stage comprising:

a current source;

a first differential transistor having a source, gate, and drain, wherein the source of the first differential transistor is coupled to the current source;

a second differential transistor having a source, gate, and drain, wherein the source of the second differential transistor is coupled to the current source;

a first series peaking inductor having positive and negative ends, wherein the negative end coupled of the first series peaking inductor is coupled to the gate of the first differential transistor;

a second series peaking inductor having positive and negative ends, wherein the negative end of the second series peaking inductor is coupled to the gate of the second differential transistor;

a first output resistor having positive and negative ends, wherein the negative end of the first output resistor is coupled to the drain the first differential transistor;

a second output resistor having positive and negative ends, wherein the negative end of the second output resistor is coupled to the drain of the second differential transistor;

a first shunt peaking inductor having positive and negative ends, wherein the negative end of the first shunt peaking inductor is coupled to the positive end of the first output resistor; and

a second shunt peaking inductor having positive and negative ends, wherein the negative end of the second shunt peaking inductor is coupled to the positive end of the second output resistor.

2. An amplifier stage as in claim , further comprising:

a first miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the first miller capacitance cancellation capacitor is coupled to the drain of the second differential transistor, and wherein the negative end of the first miller capacitance cancellation capacitor is coupled to the gate of the first differential transistor; and

a second miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the second miller capacitance cancellation capacitor is coupled to the drain of the first differential transistor, and wherein the negative end of the second miller capacitance cancellation capacitor is coupled to the gate of the second differential transistor.

3. An amplifier stage as in claim 1,

wherein the current source comprises a current source transistor having a gate, source, and drain;

wherein the gate of the current source transistor is coupled to a bias voltage.

4. An amplifier stage as in claim 3,

wherein the first and second differential transistors and the current source transistor comprise NMOS transistors.

5. An amplifier stage as in claim 3,

wherein the first and second differential transistors and the current source transistor comprise PMOS transistors.

6. An amplifier stage comprising:

a current source;

a first differential transistor having a source, gate, and drain, wherein the source of the first differential transistor is coupled to the current source;

a second differential transistor having a source, gate, and drain, wherein the source of the second differential transistor is coupled to the current source;

a first series peaking inductor having positive and negative ends, wherein the negative end coupled of the first series peaking inductor is coupled to the gate of the first differential transistor;

a second series peaking inductor having positive and negative ends, wherein the negative end of the second series peaking inductor is coupled to the gate of the second differential transistor;

a first shunt peaking inductor having positive and negative ends, wherein the negative end of the first shunt peaking inductor is coupled to the drain the first differential transistor;

a second shunt peaking inductor having positive and negative ends, wherein the negative end of the second shunt peaking inductor is coupled to the drain of the second differential transistor;

a first output resistor having positive and negative ends, wherein the negative end of the first output resistor is coupled to the positive end of the first shunt peaking inductor; and

a second output resistor having positive and negative ends, wherein the negative end of the second output resistor is coupled to the positive end of the first shunt peaking inductor.

7. An amplifier stage as in claim 6, further comprising:

a first miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the first miller capacitance cancellation capacitor is coupled to the drain of the second differential transistor, and wherein the negative end of the first miller capacitance cancellation capacitor is coupled to the gate of the first differential transistor; and

a second miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the second miller capacitance cancellation

capacitor is coupled to the drain of the first differential transistor, and wherein the negative end of the second miller capacitance cancellation capacitor is coupled to the gate of the second differential transistor.

8. An amplifier stage as in claim 6,

wherein the current source comprises a current source transistor having a gate, source, and drain;

wherein the gate of the current source transistor is coupled to a bias voltage.

9. An amplifier stage as in claim 8,

wherein the first and second differential transistors and the current source transistor comprise NMOS transistors.

10. An amplifier stage as in claim 8,

wherein the first and second differential transistors and the current source transistor comprise PMOS transistors.

11. A multi-stage differential amplifier comprising:

a first amplifier stage having a positive signal input, a negative signal input, a positive signal output, and a negative signal output; and

a last amplifier stage having a positive signal input, a negative signal input, a positive signal output, and a negative signal output;

wherein the positive signal output of the first amplifier stage is coupled to the positive signal input of the last amplifier stage, and wherein the negative signal output of the first amplifier stage is coupled to the negative signal input of the last amplifier stage;

wherein one of the first amplifier stage and last amplifier stage includes a first pair of series peaking inductors; and

wherein one of the first amplifier stage and last amplifier stage includes a first pair of shunt peaking inductors.

12. A multi-stage differential amplifier as in claim 11,
wherein one of the first amplifier stage and last amplifier stage includes a first pair of miller capacitance cancellation capacitors.

13. A multi-stage differential amplifier as in claim 12,
wherein the first amplifier stage includes the first pair of series peaking inductors, the first pair of shunt peaking inductors, and the first pair of miller capacitance cancellation capacitors.

14. A multi-stage differential amplifier as in claim 13,
wherein the last amplifier stage includes at least one pair from among a second pair of series peaking inductors, a second pair of shunt peaking inductors, and a second pair of miller capacitance cancellation capacitors.

15. A multi-stage differential amplifier as in claim 14,
wherein the last amplifier stage includes a second pair of series peaking inductors, a second pair of shunt peaking inductors, and a second pair of miller capacitance cancellation capacitors.

16. A multi-stage differential amplifier comprising:
a first amplifier stage having a positive signal input, a negative signal input, a positive signal output, and a negative signal output;
an intermediate amplifier stage having a positive signal input, a negative signal input, a positive signal output, and a negative signal output; and

a last amplifier stage having a positive signal input, a negative signal input, a positive signal output, and a negative signal output;

wherein the positive signal output of the first amplifier stage is coupled to the positive signal input of the intermediate amplifier stage, and wherein the negative signal output of the first amplifier stage is coupled to the negative signal input of the intermediate amplifier stage;

wherein the positive signal output of the intermediate amplifier stage is coupled to the positive signal input of the last amplifier stage, and wherein the negative signal output of the intermediate amplifier stage is coupled to the negative signal input of the last amplifier stage;

wherein one of the first amplifier stage, intermediate amplifier stage, and last amplifier stage includes a first pair of series peaking inductors; and

wherein one of the first amplifier stage, intermediate amplifier stage, and last amplifier stage includes a first pair shunt peaking inductors.

17. A multi-stage differential amplifier as in claim 16,

wherein one of the first amplifier stage, intermediate amplifier stage, and last amplifier stage includes a first pair of miller capacitance cancellation capacitors.

18. A multi-stage differential amplifier as in claim 17,

wherein the first amplifier stage includes the first pair of series peaking inductors, the first pair of shunt peaking inductors, and the first pair of miller capacitance cancellation capacitors.

19. A multi-stage differential amplifier as in claim 18,

wherein the last amplifier stage includes at least one pair from among a second pair of series peaking inductors, a second pair of shunt peaking inductors, and a second pair of miller capacitance cancellation capacitors.

20. A multi-stage differential amplifier as in claim 18,

wherein the intermediate amplifier stage includes at least one pair from among a second pair of series peaking inductors, a second pair of shunt peaking inductors, and a second pair of miller capacitance cancellation capacitors.

21. A multi-stage differential amplifier as in claim 18,

wherein the intermediate amplifier stage includes a second pair of series peaking inductors, a second pair of shunt peaking inductors, and a second pair of miller capacitance cancellation capacitors.

22. A multi-stage differential amplifier as in claim 21,

wherein the last amplifier stage includes a third pair of series peaking inductors, a third pair of shunt peaking inductors, and a third pair of miller capacitance cancellation capacitors.

23. A multi-stage differential amplifier comprising:

a first amplifier stage having a positive signal input, a negative signal input, a positive signal output, and a negative signal output;

a plurality of intermediate amplifier stages, the plurality having a positive signal input, a negative signal input, a positive signal output, and a negative signal output; and

a last amplifier stage having a positive signal input, a negative signal input, a positive signal output, and a negative signal output;

wherein the positive signal output of the first amplifier stage is coupled to the positive signal input of the plurality of intermediate amplifier stages, and wherein the negative signal output of the first amplifier stage is coupled to the negative signal input of the plurality of intermediate amplifier stages;

wherein the positive signal output of the plurality of intermediate amplifier stages is coupled to the positive signal input of the last amplifier stage, and wherein the negative signal output of the plurality of intermediate amplifier stages is coupled to the negative signal input of the last amplifier stage;

wherein one of the first amplifier stage, plurality of intermediate stages, and last amplifier stage includes a first pair of series peaking inductors; and

wherein one of the first amplifier stage, plurality of intermediate amplifier stages, and last amplifier stage includes a first pair of shunt peaking inductors.

24. A multi-stage differential amplifier as in claim 23,

wherein one of the first amplifier stage, plurality of intermediate amplifier stages, and last amplifier stage includes a first pair of miller capacitance cancellation capacitors.

25. A multi-stage differential amplifier as in claim 24,

wherein the first amplifier stage includes the first pair of series peaking inductors, the first pair of shunt peaking inductors, and the first pair of miller capacitance cancellation capacitors.

26. A multi-stage differential amplifier as in claim 25,

wherein the last amplifier stage includes at least one pair from among a second pair of series peaking inductors, a second pair of shunt peaking inductors, and a second pair of miller capacitance cancellation capacitors.

27. A multi-stage differential amplifier as in claim 26,

wherein one of the plurality of intermediate amplifier stages includes at least one pair from among a second pair of series peaking inductors, a second pair of shunt peaking inductors, and a second pair of miller capacitance cancellation capacitors.

28. A multi-stage differential amplifier as in claim 25,

wherein the last amplifier stage includes a second pair of series peaking inductors, a second pair of shunt peaking inductors, and a second pair of miller capacitance cancellation capacitors.

29. A multi-stage differential amplifier as in claim 28, wherein each of the plurality of intermediate amplifier stages includes a pair of series peaking inductors, a pair of shunt peaking inductors, and a pair of miller capacitance cancellation capacitors.